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EXAMINER	
VU, QUANG D	

ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,308	NARASIMHA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-9 and 11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-9 and 11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 6-9 and 11-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 6,063,681 to Son in view of US Patent No. 6,187,643 to Borland.

Regarding claim 1, Son (figures 3A-H) teaches a method for forming a low resistance MOSFET device comprising the steps of:

forming a gate region (25) atop a surface of substrate (21);

forming first spacers (26) having a first spacer width on sidewalls of the gate region (25);

forming first silicide regions (29) having a first silicide thickness (100 – 200 Angstroms; column 3, lines 58-63) in the substrate (21) as well as atop a surface of the gate region (25);

forming second spacers (31) having a second width greater than the first spacer (26) width (figure 3H) on the substrate (21), wherein the second spacers (31) protect the first silicide region (29) in the substrate (21); and

forming second silicide regions (33) in the substrate (21) and atop a surface of the gate region (25), wherein the second silicide regions (33; 100 – 300 Angstroms; column 4, lines 1-8) have a thickness that is greater than the first silicide thickness (29; 100 – 200 Angstroms).

Son differs from the claimed invention by not showing forming a dopant region comprising source/drain extensions and deep source/drain regions using a single dopant implant step. However, Borland teaches forming the source/drain extensions and the source/drain regions using single implant (column 7, lines 44-47). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Borland into the method taught by Son in order to reduce the encroachment of implant to the channel region.

Regarding claim 6, the combined device differs from the claimed invention by not showing the first spacer width is from about 5nm to about 20 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first spacer width is from about 5nm to about 20 nm in order to protect the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 7, the combined device differs from the claimed invention by not showing the first spacer width is from about 7 nm to about 15 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first spacer width is from about 7 nm to about 15 nm in order to protect the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 8, the combined device differs from the claimed invention by not showing the second spacers width is from about 20 nm to about 90 nm. It would have been

obvious to one having ordinary skill in the art at the time the invention was made for the second spacers width is from about 20 nm to about 90 nm in order to protect the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 9, the combined device differs from the claimed invention by not showing the second spacers width is from about 30 nm to about 70 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the second spacers width is from about 30 nm to about 70 nm in order to protect the gate electrode. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 11, the combined device shows the single dopant implant comprises ion implantation (Borland; n-type [As, Phosphorous]; As or Phosphorous is a type V element) of a type V element into the substrate.

Regarding claim 12, the combined device shows forming of the first silicide region (Son; 29) comprises depositing a first metal layer (Son; 28) upon an exposed surface of the substrate (Son; 21) and annealing (Son; column 3, lines 58-62).

Regarding claim 13, the combined device differs from the claimed invention by not showing the first metal layer has a thickness from about 2 nm to about 7 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the first metal layer has a thickness from about 2 nm to about 7 nm in order to increase the conductivity

of metal layer. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 14, the combined device shows the first metal layer (Son; 28) comprises Ti (Son; column 4, lines 5-6).

Regarding claim 15, the combined device shows the thickness of the first silicide region (Son; 29) is 10-20 nm (100 – 200 Angstroms) (Son; 100-200 Angstroms; column 3, lines 58-62), which is in the range (1 – 20 nm) of the claimed invention.

Regarding claim 16, the combined device shows the thickness of the first silicide region (Son; 29) is 100 – 200 Angstroms (10 – 20 nm) (Son; 100-200 Angstroms; column 3, lines 58-62), which is in the range (2 – 15 nm) of the claimed invention.

Regarding Claim 17, the combined device shows the thickness of the first silicide region (Son; 29) is 100 – 200 Angstroms (10 – 20 nm) (Son; 100-200 Angstroms; column 3, lines 58-62), which is in the range (5 –12 nm) of the claimed invention.

Regarding claim 18, the combined device shows the first silicide region (Son; 29) is formed in the substrate (Son; 21) having a channel region (Son; a portion of region is located under the gate and between the source/drain extension regions [27]) beneath the gate region.

The combined device differs from the claimed invention by not showing the distance between the first silicide region and the channel region is from about 2 nm to about 15 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the distance between the first silicide region and the channel region is from about 2 nm to about 15 nm in order to increase the speed of the device. Furthermore, it has been held that

where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 19, the combined device shows the first silicide region (Son; 29) is formed in the substrate (Son; 21) having a channel region (Son; a portion of region is located under the gate and between the source/drain extension regions [27]) beneath the gate region.

The combined device differs from the claimed invention by not showing the distance between the first silicide region and the channel region is form about 3 nm to about 10 nm. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the distance between the first silicide region and the channel region is form about 3 nm to about 10 nm in order to increase the speed of the device. Furthermore, it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

3. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Son in view of Borland, and further in view of US Patent No. 6,313,020 to Kim et al.

The disclosures of Son and Borland are discussed as applied to claims 1, 6-9 and 11-19 above.

Regarding claim 2, the combined device differs from the claimed invention by not showing the forming of the gate region further comprises predoping of the gate region. However, Kim et al. teach forming of the gate region comprising predoping process (column 1, lines 26-34). Therefore, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to incorporate the teaching of Kim et al. into the device taught by Son in order to improve the level of the electrons in the gate region.

Regarding claim 3, the combined device shows the predoping is preformed by ion implantation of a type III-A element (Kim et al.; Boron is III-A element; column 1, lines 30-34).

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Son and Borland in view of Kim et al., and further in view of US Patent No. 6,399,452 to Krishnan et al.

Regarding claim 4, the disclosures of Son, Borland and Kim et al. are discussed as applied to claims 2 and 3 above.

The combined device differs from the claimed invention by not showing predoping is achieved via ion implantation of phosphorus into the gate region. However, Krishnan et al. teach predoping is achieved by implantation of phosphorus into the gate (column 2, lines 42-53). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Krishnan et al. into the method taught by Son, Borland and Kim et al. in order to improve the level of the electrons in the gate region.

Response to Arguments

Applicant's arguments filed 09/27/04 have been fully considered but they are not persuasive.

It is argued, in page 8 of the remarks, that Son does not teach or suggest forming a dopant region comprising source/drain extensions and deep source/drain regions using a single dopant implant. This argument is not convincing because the combined device (Son and Borland)

shows forming a dopant region comprising source/drain extensions and deep source/drain regions using a single dopant implant for the reason that is discussed above.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 571-272-1667. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

qv
December 9, 2004

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